OBC lite™ 52X series

- Fully compatible with Space Plug-and-Play Avionics (SPA) network protocol layer SPA-U and SPA-1 – 'SPAready'. Compliant with the Low Voltage SPA (LV-SPA) power subset standard (5 V)
- Fast, easy integration of high data rate or computationally-demanding payloads and sub-systems using products in the Rapid Integration Architecture™ (RIA) family
- Runs Linux Operating System on ÅAC Microtec OpenRISC Fault Tolerant™ 32-bit CPU
- Runs a complete PnP Manager (Satellite Data Model [SDM], Satellite System Manager [SSM] or similar)

Robust and failure-tolerant onboard computer

ÅAC Microtec OpenRISC M model (EM) and OpenRISC Fault Tolerant™ M model (FM) processors and microcontroller platforms currently consist of two families: the On-Board Computer (OBC) series and the Remote Terminal Unit (RTU) series. Both provide advanced integrated safety features designed specifically for safety critical applications. They also offer options for performance, connectivity, safety features, and memory.

OBC application focus

OBCs provide advanced capabilities for reliably controlling and integrating an autonomous vehicle or system.

The OBC lite™ family delivers high performance for safety applications based on ÅAC Microtec's OpenRISC Fault Tolerant™ M (ORFT-M) processor.

Key industrial markets include:

- Space
- Avionics and defense applications
- Industrial automation and control
- Turbines and windmills
- Power generation and distribution
- Motor control
- Off-highway vehicles

OBC lite™ 52X series is a compact, high-density On-Board Computer (OBC) family for autonomous robots and probes such as satellites and Unmanned Aerial Vehicles (UAVs). Its applications also include embedded systems that feature a powerful fault-tolerant ÅAC Microtec 32-bit OpenRISC Fault Tolerant™ M processor (FM), as well as peripherals for robust operation.

The series provides simple user integration as well as general support for fast speed 10/100 T-base Ethernet, USB device, I2C, SPI, analog and General Purpose IO. In addition, users can select support for ÅAC Microtec's Rapid Integration Architecture™ (RIA) based on Space Plug-and-Play Avionics (SPA) standards.

OBC lite™ 52X products are all compatible with ÅAC Microtec Rapid Integration Architecture™ (RIA) and support health-monitoring for advanced Fault Detection, Isolation and Recovery (FDIR) functionality. This means that user software can detect problems and take appropriate action to save the system.

Figure 1 shows the OBC lite™ 521 hardware. Figure 2 highlights the basic user connectivity options.

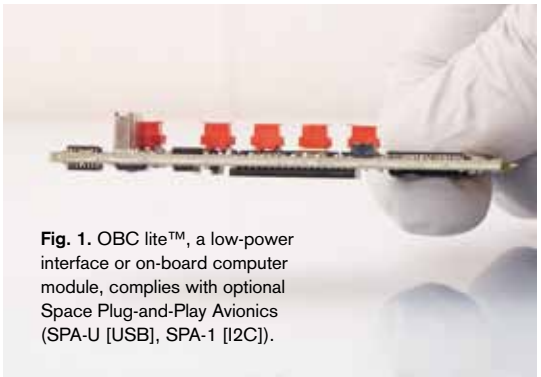

Fig. 1. OBC lite™, a low-power interface or on-board computer module, complies with optional Space Plug-and-Play Avionics (SPA-U [USB], SPA-1 [I2C]).

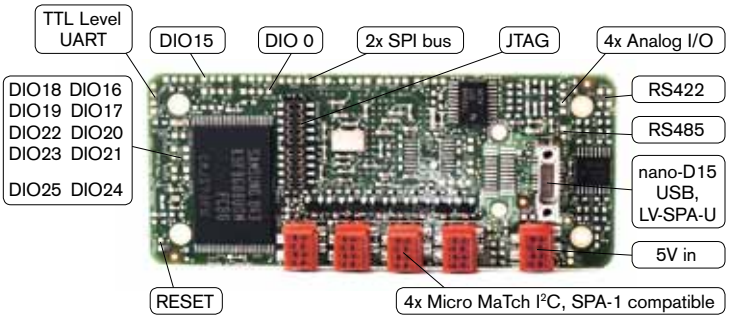

Fig. 2. OBC Lite™ 521 with description of the main I/O:s.

Thanks to its many interfaces, OBC lite™ also has a wide range embedded applications. Moreover, in addition to its use with the SPA standard, OBC lite™ performs many distributed tasks as a stand-alone device. It also acts as a Plug-and-Play Network Manager in smaller systems.

Space Plug-and-Play Avionics (SPA) compatible

OBC lite™ has been developed together with the US Air Force Research Laboratory (AFRL), the Swedish Defence Materiel Administration (FMV), and the Swedish National Space Board (SNSB).

The device is SPAready. However, to reduce software overheads, it can easily be run with custom-user protocols without enabling SPA.

SPA is defined as an interface-driven set of standards encompassing hardware, software and protocols intended to promote the rapid, affordable design and integration of spacecraft busses and payloads. SPA standards combine different data transport standards, such as USB (SPA-U), SpaceWire (SPA-S) and I2C (SPA-1) with a component-transparent publish/subscribe software infrastructure called the Satellite Data Model (SDM). Command, control, data collection, processing and analysis software can all be implemented on SDM.

When the device is used in Plug-and-Play operation, an electronic data sheet called the extended Transducer Electronic Data Sheet (xTEDS) is stored with each SPA component. xTEDSs contain descriptions of all component-specific commands accepted, variables produced, and data messages that can be delivered. Thanks to these standardized elements, a Plug-and-Play system can be rapidly designed and integrated from off-the-shelf SPAready components. Figure 3 shows device examples of ÅAC Microtec SPAready RTUs and OBCs.

Architecture

OBC lite™ also features an advanced set of IP blocks configured for implementation in FPGA (see Fig. 4).

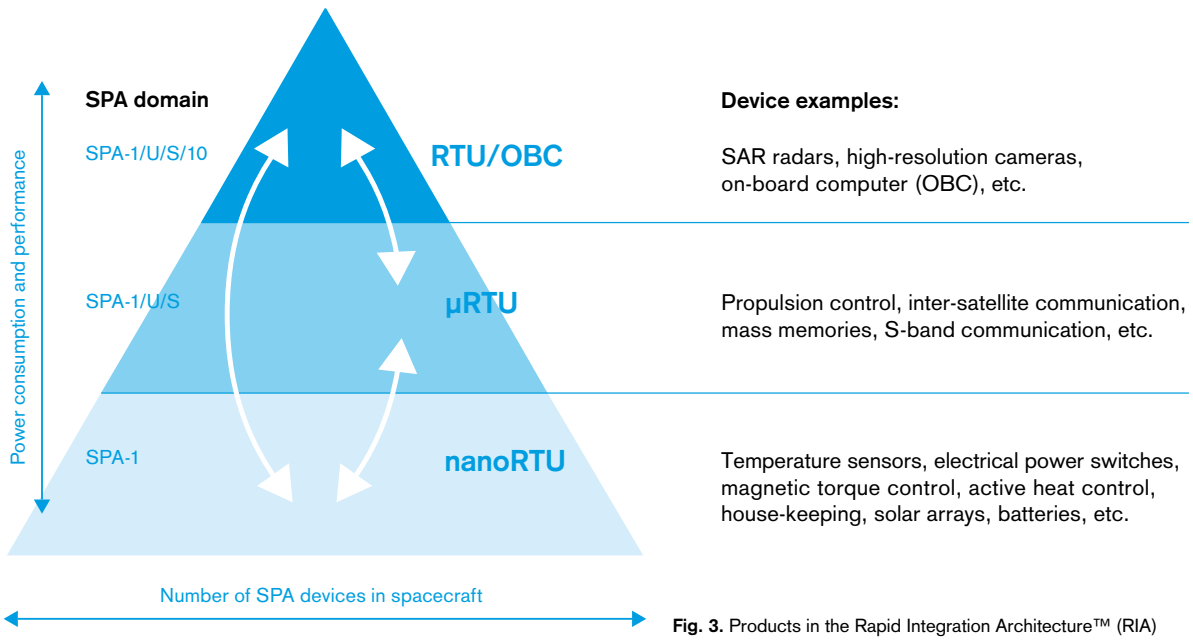

Fig. 3. Products in the Rapid Integration Architecture™ (RIA) family showing the numbers and types of SPAready RTU/OBC devices that can be found in a spacecraft.

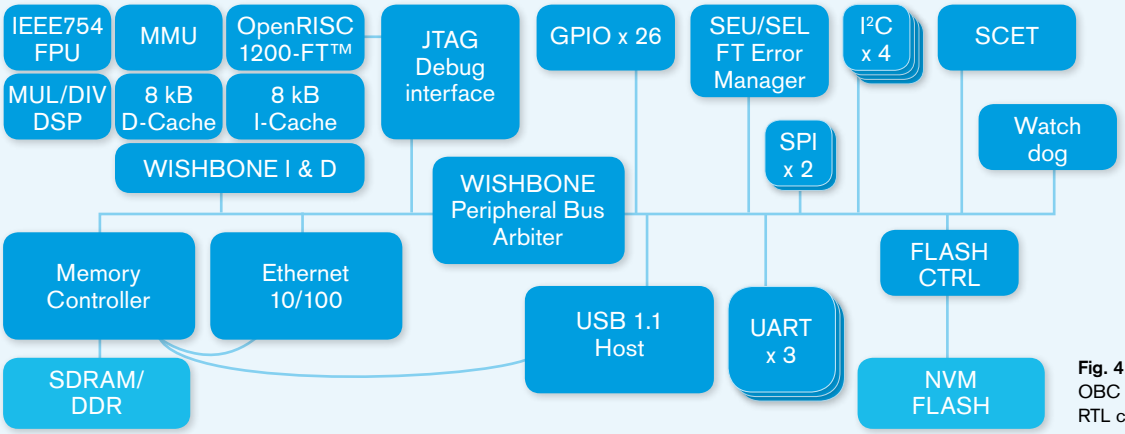

Fig. 4.
OBC lite™ FPGA RTL configuration.

ÅAC Microtec OpenRISC processors have extensive development support tools:

- CGEN
- Binutils 2.22.0
- GCC 4.5.3 with C and C++ support
- GDB 7.2 for target debugging
- Newlib 1.18.0
- µClibc 0.9.32
- Universal bootloader
- OpenOCD JTAG debug interface
- OR1ksim Architecture simulator

OBC lite™ can run either bare metal code compiled with newlib or code for OpenRISC Linux based on µClibc.

Linux operating systems are available for the OpenRISC architecture. Linux 3.2 or later are supported and maintained by ÅAC Microtec. Key features of the OpenRISC LINUX port include:

- Updated Device handling – the new way to define platform devices via a device tree description.
- Extended CPUINFO reporting – adds many new cpuinfo reporting items.
- Kernel clean-up.
- Better time management and high-resolution timers.
- Assembly optimization for OpenRISC.
- Improved Commandline handling – gets the DEFAULT_CMDLINE option in the kernel configuration working.
- Improved bit field searching using OpenRISC instructions l.ff1 and l.fl1.

Engineering and flight models

Engineering model (EM) is for development in a lab environment only. Flight model (FM) is designed according to the ECSS-Q-30-11A EEE component derating standard. Comprehensive SEE/SEU hardware protection is provided.

Programming interface equipment and tools

OBC lite™ is programmed through the supplied Universal bootloader and ÅAC Microtec JTAG and UART interfaces. Firmware loading is via Ethernet, USB or serial ports. Figure 5 shows an overview of the Ethernet interface board that is assembled on top of OBC lite™ (EM).

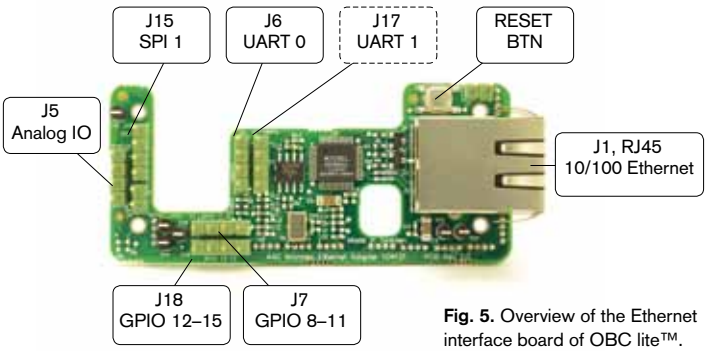

Fig. 5. Overview of the Ethernet interface board of OBC lite™.

Technical specifications – OBC lite™ 52X series

KEY PARAMETERS	
Processor	32 bit OpenRISC Fault Tolerant™ M processor (FM) 32 bit OpenRISC M processor (EM)
Processor clock	18 MHz
SCET	136 years, resolution15.3 µ s (Min)
SDRAM	64 MB (EM) and 40 MB (FM)
Instruction cache	8 kB
Data cache	8 kB
Mass storage	1 GB NAND parallel FLASH
Communication	4 x I2C master/slave busses with pull-ups (100 kbps, 400 kbps) 2 x SPI master 1 x USB 1.1 Host, 12 Mbps w/DMA 1 x Ethernet 10/100 Mbps w/ DMA 1 x RS422 1 x RS485 JTAG real-time debug interface (OpenOCD)
SPA capabilities	4 x SPA-1 1 x LV-SPA-U
Total Ionizing Dose	20 krad component level (FM)
ANALOG INPUT	
Number of AD channels	4 (shared with DA)
AD resolution	12 bit
AD sampling rate	100 kSps
Input voltage range	0–2 Vpp
Bandwidth	50 kHz
ANALOG OUTPUT	
Number of DA channels	4 (shared with AD)
DA resolution	12 bit
DA refresh period	200 kHz
Output voltage level	0–3.3 Vpp
Bandwidth	100 kHz
Impedance	2 kΩ
GPIO	
Number of GPIO	26
Output/input	3.3 V – TTL
CONNECTOR	
PCB connector (EM)	SPA-1, Micro-MaTch 4 LV-SPA-U, 1 x 15 pins nano D Power in, Micro-MaTch 4 Ethernet, RJ45
PCB connector (FM)	SPA-1, Pico-EZmate™ 4 LV-SPA-U, 1 x 15 pins nano D Power in, Pico-EZmate™ 5
POWER SUPPLY	
Supply voltage	5 V
Power consumption	1.5 W nominal power consumption
User power	12.5W (2.5A @ 5V)

DIMENSIONS	
PCB OBC	70 × 30 x 10 mm
Ethernet board	71 x 32 x 21 mm
WEIGHT	
PCB OBC	15 gram
ENVIRONMENTAL	
Operating temperature	-40 to +60°C
Storage temperature	-20 to +70°C
Relative humidity, non-condensing	5%–95%

FAULT-TOLERANT IMPLEMENTATION

OBC lite™ Flight Model (FM) features advanced fault tolerance, the main aspects of which are summarized below:

- Components on the board are derated according to ESA ECSS standards
- All BGA soldering interfaces are inspected with 3D X-ray
- Continuous EDAC scrubbing of SDRAM with 1-bit error correction and 2-bit error detection on each 32-bit instruction. Non-correctable error causes user interrupt and action.
- EDAC checking of instructions before execution (1-bit error correction and 2-bit error detection on each 32-bit instruction). Non-correctable error causes automatic reboot.
- Parity checking of Instruction and Data caches. Error causes cache reload.
- Parity checking of peripheral FIFOs.
- Triple Modular Redundancy (TMR) on all FPGA flip-flops
- Triple Modular Redundancy (TMR) on boot flash
- FPGA SEU bank flip detection. Bank SEU leads to automatic reboot of the device.
- FPGA Clock skew detection. Clock skew leads to automatic reboot of the device.
- Watchdog. Watchdog tripping leads to automatic reboot of the device.
- Advanced error manager counts and stores detected failures during reset/reboot for later analysis.

HEALTH MONITORING	
Interface temperature precision	1 °C
Input voltage precision	0.1 V
Input current precision	10 mA
User 3.3 V regulated precision	0.1 V

APPLICATION SOFTWARE / BOARD SUPPORT PACKAGE

- API Library (C and C++ Application Programming)
- Interface driver library
- Linux 3.2 source code
- Satellite Data Model programming API

COMPLIANCE	LV-SPA-U and SPA-1

ORDER INFORMATION

Part number	Item	Description
104110	OBC lite™ 521	Engineering Model (EM)
104111	OBC lite™ 522	Flight Model (FM)
104127	OBC lite™ 521	Development Kit (EM)

For more information, please contact:
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