Remote Terminal Unit μRTU™ 300 series

- Fully compatible with Space Plug-and-play Avionics (SPA) network protocol layer for SPA-S, SPA-U and SPA-1 – 'SPAready'. Compliant with the Low Voltage SPA (LV-SPA) power subset standard (5 V)
- Supports SPA network bridging (SPA-1 to SPA-S and SPA-1 to SPA-U)
- Fast, easy integration of high data rate or computational-demanding payloads and sub-systems

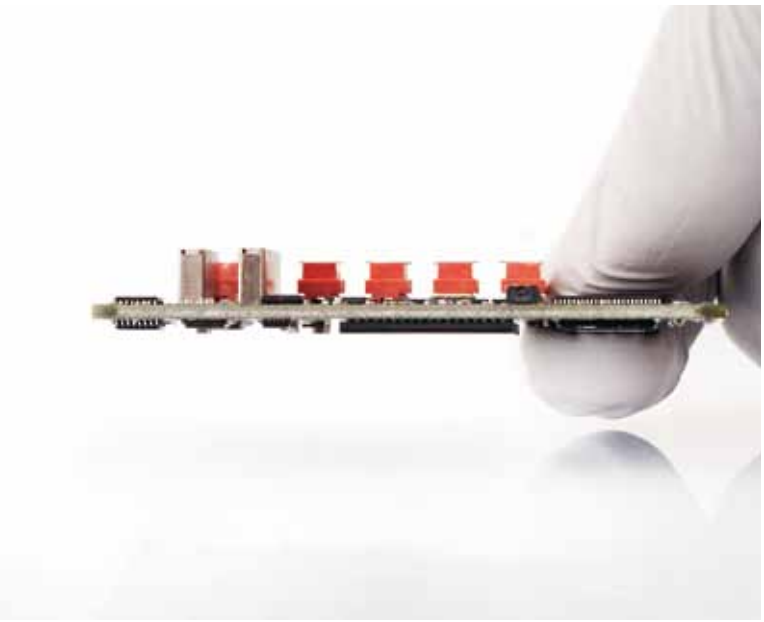

FIG. 1. μRTU™ is a low-power interface module with Space Plug-and-play Avionics (SPA-S [SpaceWire], SPA-U [USB], SPA-1 [I²C]) compliance. Its many interfaces allow numerous embedded applications.

Versatile interface and control computer

Remote Terminal Unit devices (RTUs), sometimes called Appliqué Sensor Interface Modules (ASIMs) or Remote Data Concentrators (RDCs), are flexible, compact high-density interface and control computers that support many common protocols and analog/digital IOs. The units are suitable for unmanned vehicles, robotics and other embedded systems (e.g. satellites or unmanned aerial/ground/water vehicles [UAV/UGV/UWV]).

RTU devices allow fast and easy integration of payloads, sensors and sub-systems on advanced systems. ÅAC Microtec products support flexible, user-friendly RTU interfaces based on cost-efficient flash-based FPGAs. The FPGA platform allows either standard ÅAC Microtec-supplied hardware RTL or hardware accelerated with user-IP compatible with WISHBONE B3. Both are perfect for interfacing electronic devices and payloads.

In addition to its use with the SPA standard, μRTU™ can perform many distributed tasks as a stand-alone device.

In providing SPA-S, SPA-U and SPA-1 compatibility, key μRTU™ applications include:

- Support to legacy sub-systems, sensors and actuators
- Propulsion control
- Inter-satellite communication
- Mass memories
- S-band communication

Space Plug-and-play Avionics (SPA) compatible

μRTU™ has been developed together with the US Air Force Research Laboratory (AFRL) and the Swedish Defence Materiel Administration (FMV).

Although the device is SPAready, it can easily be used with custom-user protocols without enabling SPA, which will reduce software overheads.

SPA is defined as an interface-driven set of standards encompassing hardware, software and protocols intended to promote the rapid, affordable design and integration of spacecraft busses and payloads. SPA standards combine different data

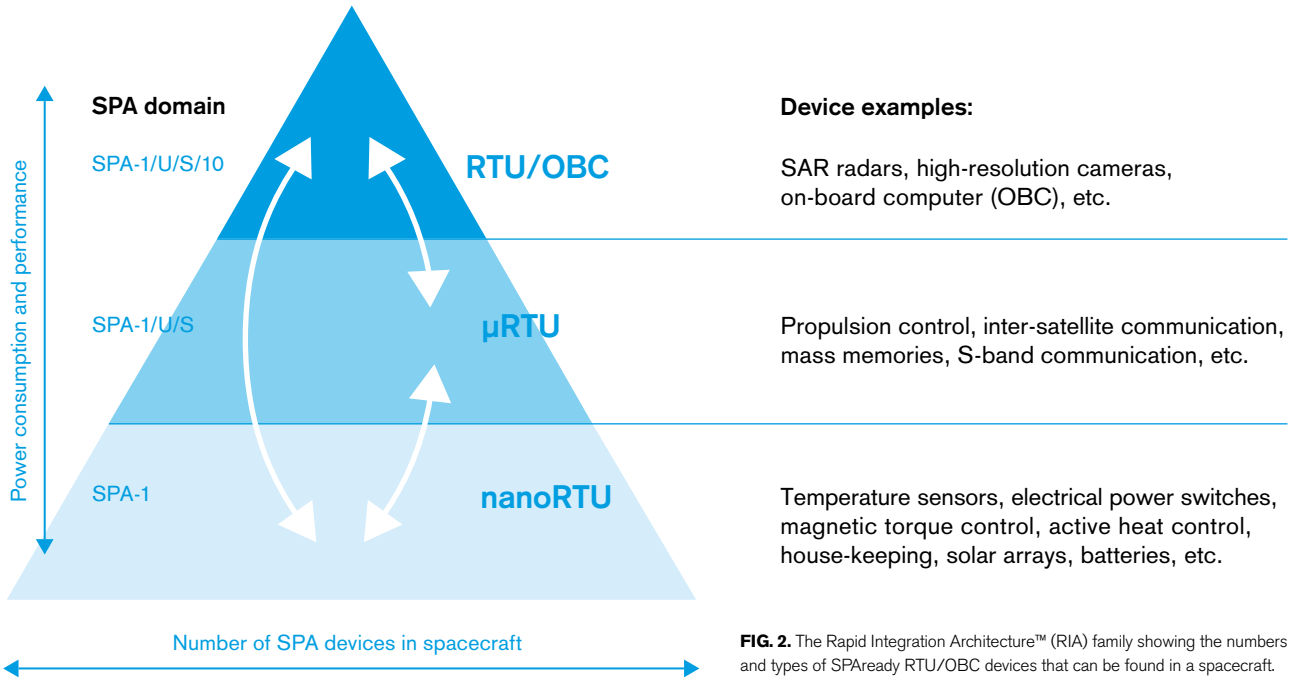

FIG. 2. The Rapid Integration Architecture™ (RIA) family showing the numbers and types of SPAready RTU/OBC devices that can be found in a spacecraft.

transport standards, such as Universal Serial Bus (USB) (SPA-U), SpaceWire (SPA-S), and I²C (SPA-1) with a component-transparent publish/subscribe software infrastructure called the Satellite Data Model (SDM), on which software for command, control, data collection, processing and analysis can be implemented.

If the device is used in plug-and-play operation, an electronic data sheet called the extended Transducer Electronic Data Sheet (xTEDS) is stored with each SPA component. This xTEDS contains descriptions of all component-specific commands accepted, variables produced and data messages that can be delivered. Thanks to these standardized elements, a plug-and-play system can be rapidly designed and integrated from off-the-shelf SPAready components. Fig. 2 shows device examples of ÅAC Microtec SPAready RTUs/OBCs.

Architecture

The μRTU™ PCB contains the SPA-S, SPA-U and SPA-1 core (FPGA) and AD/DA converters. The AD converters also support health-monitoring (house-keeping) information of critical signals. In addition, μRTU™ includes an advanced set of IP blocks configured for implementation in FPGA. See Fig. 3 for further details.

OpenRISC R-model overview

The OpenRISC R-model has extensive development support tools:

- Binutils 2.20.1
- GCC 4.5.3 with C and C++ support
- GDB 7.2 for target debugging
- Newlib 1.18.0
- OR1ksim Architecture simulator
- μRTU™ can run bare metal code compilations based on newlib and realtime operating systems such as RTEMS, eCOS and FreeRTOS.

Engineering and flight models

The engineering model (EM) is intended for development in a lab environment only. Flight model (FM) is designed according to the ECSS-Q-30-11A EEE component derating standard. Comprehensive SEE/SEU hardware protection is provided.

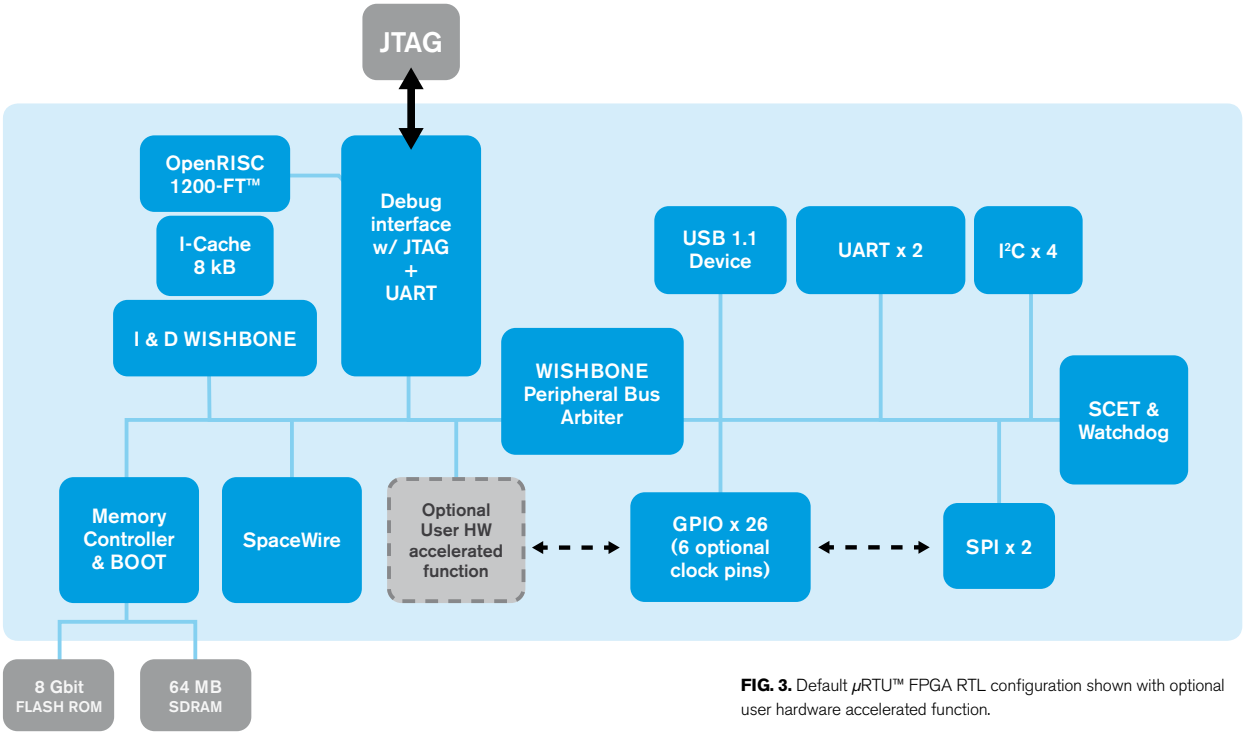

FIG. 3. Default μRTU™ FPGA RTL configuration shown with optional user hardware accelerated function.

Programming interface equipment and tools

The development environment is based on the OpenRISC GNU toolchain, which is free under the GPL license. This toolchain runs on a host PC running Ubuntu 12.04 LTS. For firmware development, any editor under Linux can be used. Compilation is done with a simple script provided with the OpenRISC toolchain. μRTU™ is programmed using the OpenRISC USB JTAG Debugger device that is controlled using GDB. As well as the possibility to program the μRTU™, GDB also offers a set of onboard debugging methods.

Features

- OpenRISC Fault Tolerant™ R model processor core supporting 1.4 DMIPS per MHz, 25 DMIPS @ 18 MHz
- Core available as radiation-tolerant FPGA
- 64 MByte RAM
- 1 GByte flash ROM storage for program and user data
- 1 x USB1.1 physical interface
- 1 x SpaceWire physical interface
- 4 × I²C physical interface
- 26 x General Purpose IO (GPIO)
- 2 × UART
- Internal health-monitoring
  - Input voltage level (V)
  - Input current level (A)
  - Module temperature (°C)
  - Internal voltage level (V)
- Approx. 1 W nominal power consumption

Features may be supported on different models. Check technical specifications.

Software support

API C library
ÅAC Microtec sample application code

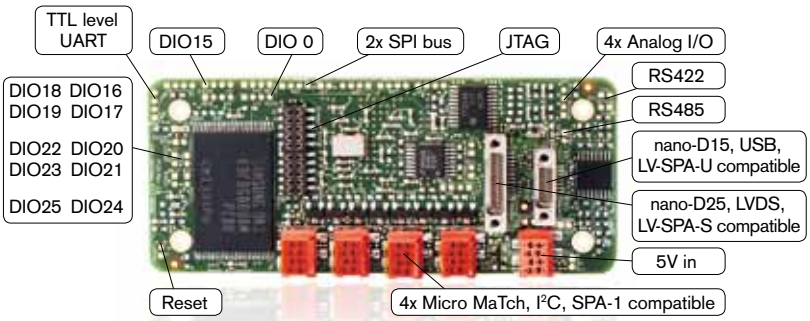

FIG. 4. μRTU™ overview.

Technical specifications – Remote Terminal Unit μRTU™

KEY PARAMETERS	
Processor	32 bit OpenRISC Fault Tolerant™ R processor (FM) 32 bit OpenRISC R processor (EM)
Processor clock	18 MHz
SCET	136 years, resolution15.3 μs (Min)
RAM	64 MB
Memory (ROM)	1 GB
Communication	4 × I²C (100 kbps or 400 kbps) 2 × UART 1 × USB 1.1 (12 Mbps), device only 1 × SpaceWire (10 Mbps) 2 × SPI 1 × RS-422 1 × RS-485 2 × LVDS
SPA capabilities	4 × SPA-1 1 × LV-SPA-U 1 × LV-SPA-S
Total Ionizing Dose	20 krad component level (FM)
ANALOG INPUT	
Number of AD channels	4 (shared with DA)
AD resolution	12 bit
AD sampling rate	100 kSps
Input voltage range	0–2 Vpp
Bandwidth	50 kHz
ANALOG OUTPUT	
Number of DA channels	4 (shared with AD)
DA resolution	12 bit
DA refresh period	200 kHz
Output voltage level	0–3.3 Vpp
Bandwidth	100 kHz
Impedance	2 kΩ
GPIO	
Number of GPIO	26 (of which 6 can be used as clock input)
Output/input	3.3 V – TTL
CONNECTOR	
PCB connectors EM	SPA-1, 4 × Micro-MaTch 4 LV-SPA-U, 1 × 15 pins nanoD LV-SPA-S, 1 × 25 pins nanoD Power in, 1 × Micro-MaTch 4
PCB connectors FM	SPA-1, 4 × Pico-EZmate 4 LV-SPA-U, 1 × 15 pins nanoD LV-SPA-S, 1 × 25 pins nanoD Power in, 1 × Pico-EZmate 5

POWER SUPPLY	
Supply voltage	5 V
Power consumption	1.5 W
User power	12.5W (2.5A @ 5V)
DIMENSIONS	
PCB	70 × 30 x 10 mm
WEIGHT	
PCB	15 gram
ENVIRONMENTAL	
Storage temperature	-40–+85 °C
Operating temperature	-40–+60 °C
Relative humidity, non-condensing	5%–95%

FAULT DETECTION & CORRECTION

μRTU™ Flight Model (FM) features advanced fault tolerance, the main aspects of which are summarized below:

- All components on the board are derated according to ESA ECSS standards
- All BGA soldering interfaces are inspected with 3D X-ray
- Continuous EDAC scrubbing of SDRAM with 1-bit error correction and 2-bit error detection on each 32-bit instruction. Non-correctable error causes user interrupt and action.
- EDAC checking of instructions before execution (1-bit error correction and 2-bit error detection on each 32-bit instruction). Non-correctable error causes automatic reboot.
- Parity checking of Instruction and Data caches. Error causes cache reload.
- Parity checking of peripheral FIFOs.
- Triple Modular Redundancy (TMR) on all FPGA flip-flops
- Triple Modular Redundancy (TMR) on boot flash
- FPGA SEU bank flip detection. Bank SEU leads to automatic reboot of the device.
- FPGA Clock skew detection. Clock skew leads to automatic reboot of the device.
- Watchdog. Watchdog tripping leads to automatic reboot of the device.
- Advanced error manager counts and stores detected failures during reset/reboot for later analysis.

HEALTH MONITORING	
Interface temperature precision	1 °C
Input voltage precision	0.1 V
Input current precision	10 mA
User 3.3 V regulated precision	0.1 V
APPLICATION SOFTWARE	
API Library	C Application Programming Interface driver library
COMPLIANCE	LV-SPA-S, LV-SPA-U and SPA-1

ORDER INFORMATION

Part number	Item	Description
104106	μRTU™ 311	Engineering Model (EM)
104109	μRTU™ 312	Flight Model (FM)
104126	μRTU™ 311	Development kit (EM)

For more information, please contact:
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